

PATENT ABSTRACTS OF JAPAN

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(71)Applicant : FURUKAWA ELECTRIC CO LTD:THE

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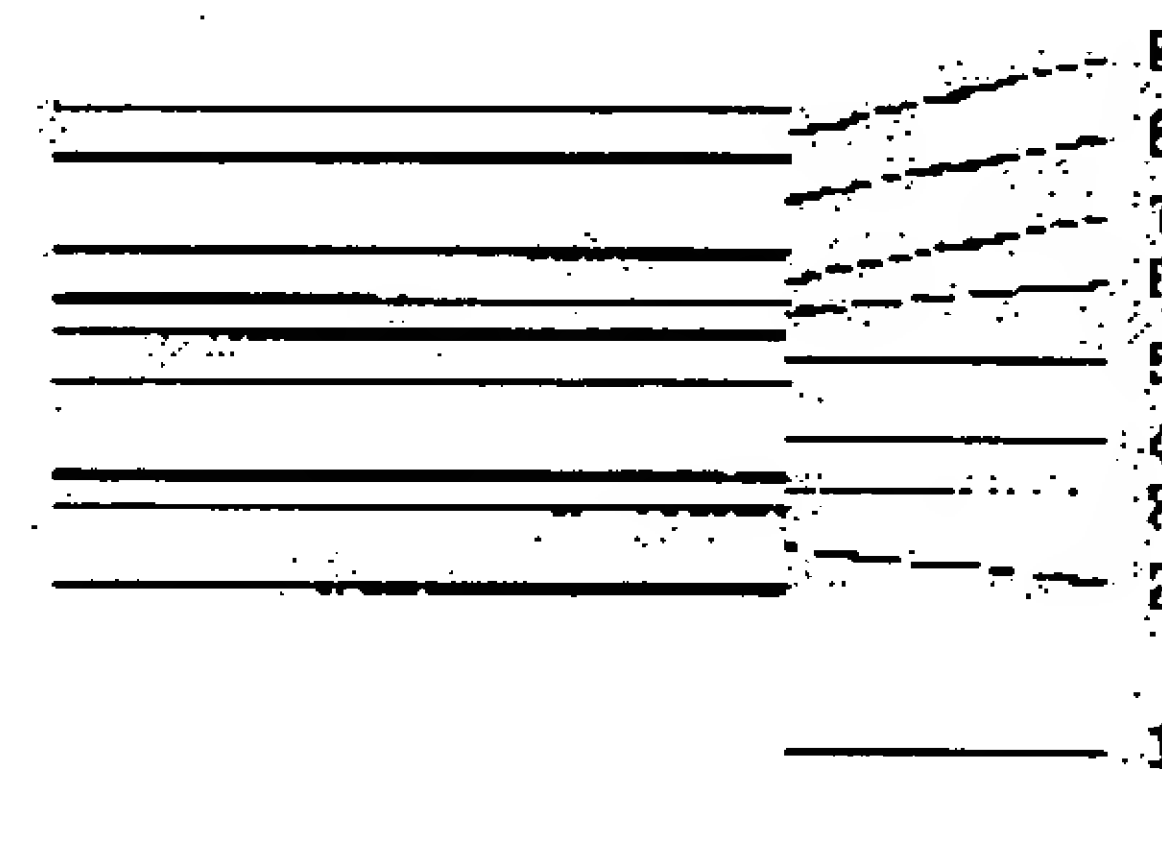
(72)Inventor : SHIMIZU HITOSHI

(54) METHOD FOR GROWING GROUP III-IV SEMICONDUCTOR THIN FILM

(57)Abstract:

PURPOSE: To grow the crystal of a group III-V semiconductor with excellent crystallinity by providing at least one crystalline layer which is grown while its crystal face is maintained on the stabilized surface of a group III element and has a thin thickness which falls within a specific range in a semiconductor thin film.

CONSTITUTION: The thickness of a thin crystalline layer which is grown while its crystal face is maintained on the stabilized surface of a group III element is limited to $\geq 1\mu\text{m}$ so as to prevent the degree of flattening from becoming insufficient, because the degree becomes insufficient due to the migration of the group III element when the thickness is thin. In addition, the thickness of the crystal face growing layer of the group III element is limited to $\leq 200\text{nm}$ so as to prevent the dropping degree of surface morphology of crystal. Moreover, when one face growing layer of the group III element is introduced, the flatness and crystallinity of the semiconductor crystal layer which grows thereafter are improved.



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CLAIMS

[Claim(s)]

[Claim 1] The growth approach of the 3-5 group semi-conductor thin film characterized by preparing at least one layer of thin film crystal layers of 1-200nm of thickness which grew holding a crystal front face in this semi-conductor thin film in 3 group stabilization side on a semi-conductor substrate in the growth approach of a semi-conductor thin film of performing crystal growth, holding the 3-5 group semiconducting crystal front face under growth to 5 group stabilization side.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the approach of carrying out crystal growth of the 3-5 group semiconductor thin film of high quality on a semi-conductor substrate.

[0002]

[Description of the Prior Art] As for the ingredient of the InGaAs/InAlAs system which carries out lattice matching to InP, band structure is suitable for the light receiving and emitting element for optical communication of 1.3-1.55-micrometer band. Moreover, since the electron mobility of InGaAs is about 2 times large as compared with GaAs, it is expected as a next-generation electron device ingredient. For this reason, the approach of carrying out crystal growth of InGaAs/InAlAs which is excellent in surface smoothness and crystallinity on current and an InP substrate is studied briskly.

[0003] general — MBE — law and MOCVD — if there is little amount of supply of 5 group element when carrying out crystal growth of the 3-5 group semi-conductor by law etc., 5 group element with high vapor pressure will break away out of a crystal, and surface morphology will fall. For this reason, the crystal growth of a 3-5 group semi-conductor supplies 5 group element superfluously, and where the crystal front face under growth is maintained at 5 group stabilization side, it is performed.

[0004] However, when carrying out crystal growth of InGaAs/InAlAs on an InP substrate, there is a problem that the surface smoothness of a crystal and crystallinity cannot be enough raised only by holding the crystal front face at the time of growth to 5 group stabilization side. Since band offset ΔE_c of the valence band in InGaAs/InAlAs quantum well structure is specifically higher than the InP/InGaAsP quantum well structure where $0.7\Delta E_g$ (bandgap energy difference $\Delta E_g=0.70\text{eV}$) and ΔE_c are $0.4\Delta E_g(s)$ ($\Delta E_g=0.59\text{eV}$), it is thought theoretically that the MQW semiconductor laser of an InGaAs/InAlAs system is oscillated with a low threshold rather than the MQW semiconductor laser of an InP/InGaAsP system. Nevertheless, since it was difficult on an InP substrate to grow up the InGaAs/InAlAs crystal which is excellent in surface smoothness and crystallinity, the threshold current density (about three 2.4 kA/cm) of the MQW semiconductor laser of the conventional InGaAs/InAlAs system was inferior as compared with the threshold (about three 1.0 kA/cm) of the MQW semiconductor laser of an InP/InGaAsP system.

[0005] By the way, there is the approach of introducing a superlattice buffer layer into a crystal layer as a means to improve the surface smoothness of an InGaAs/InAlAs crystal which grows on an InP substrate, and crystallinity (Matthews: JP,48-20762,A). Drawing 2 is the explanatory view showing the epitaxial structure of the MQW semiconductor laser which introduced the superlattice buffer layer.

[0006] An n mold InP substrate and 12 11 among drawing 2 The n mold InAlAs buffer layer of 0.5 micrometers of thickness, The n mold InAlAs cladding layer of 1 micrometer of thickness and 15 14 The p mold InAlGaAs-SCH layer of 0.15 micrometers of thickness, 16 Well width of face of 9nm, barrier width of face of 5nm, an InGaAs/InAlAs multiplex quantum well barrier layer with six wells, The p mold InAlGaAs-SCH layer of 0.15 micrometers of thickness and 18 17 The p mold InAlAs cladding layer of 0.4 micrometers of thickness, 19 is the p+ mold InGaAs contact layer of 2 micrometers of thickness, and 13 is the superlattice buffer layer which carried out the laminating of InGaAs of 2nm of thickness, and about ten layer each of the InAlAs(es) of 2nm of thickness by turns. In addition, also in this approach, the crystal front face under growth is always maintained at 5 group stabilization side.

[0007]

[Problem(s) to be Solved by the Invention] However, since the conventional approach of introducing a superlattice buffer layer needs to grow many superlattice layers, it has thickness and the trouble that control of a presentation is difficult. Moreover, the threshold of MQW semiconductor laser shown in drawing 2 is inferior to the MQW semiconductor laser of the 2.0 kA/cm³ and InP/InGaAsP system, and it is shown that the surface smoothness of the crystal obtained by this approach and crystallinity are inadequate.

[0008] This invention solves the above-mentioned trouble and are simple and a thing aiming at offering the approach of growing up the crystal of the 3-5 group semi-conductor which excels [stability] in surface smoothness and crystallinity on a semi-conductor substrate.

[0009]

[Means for Solving the Problem] If a thin film crystal is grown up this invention holding the crystal front face under growth to 3 group stabilization side The result by which the migration of 3 group element under this thin film crystal becomes active, and the surface smoothness of this thin film crystal layer is promoted, In the growth approach of a semi-conductor thin film of performing crystal growth based on discovery that the surface smoothness of a semiconducting crystal layer which grows after that, and crystallinity are improved, holding the 3-5 group semiconducting crystal front face under

growth on a semi-conductor substrate in 5 group stabilization side. It is the growth approach of the semi-conductor thin film characterized by preparing at least one layer of thin film crystal layers of 1-200nm of thickness which grew holding a crystal front face to 3 group stabilization side into this semi-conductor thin film.

[0010] The reason which limited the thickness of a thin film crystal layer (henceforth 3 **** growth phase) which grew in this invention, holding a crystal front face to 3 group stabilization side to 1nm or more. When the thickness of 3 **** growth phase becomes thin, there is an inclination for the degree of flattening of the crystal by the migration of 3 group element to become inadequate. The reason which is because the effectiveness of this invention is no longer acquired in thickness 1nm or less, and limited the thickness of 3 **** growth phase to 200nm or less. When thickness is thickened, it is in the inclination which extent of a fall of the surface morphology of the crystal by balking of 5 group element expands, and in thickness 200nm or more, it is for the surface smoothness of a semiconducting crystal layer which grows after that, and crystallinity to fall on the contrary. So, the thickness of most desirable 3 **** growth phase is 10nm - 50nm.

[0011] Moreover, if one layer of 3 **** growth phases is introduced, the surface smoothness of a semiconducting crystal layer which grows after that, and crystallinity will fully improve, but if it is the above-mentioned range of thickness, even if it will introduce two or more 3 **** growth phases, the surface smoothness of a semiconducting crystal layer which grows after that, and crystallinity not falling, and introducing 3 **** growth phase of two or more layers is also included in the range of this invention.

[0012] In addition, the approach of controlling a crystal front face to 3 group stabilization side is well-known. That is, by raising growth temperature or decreasing 5 group element amount of supply, it is possible to make the front face of a growth phase into 3 group stabilization side, and it is good to grasp the conditions which change from 2x4 supramolecular structure to 4x2 supramolecular structure with a reflective mold high energy electron beam DI contact sense non-isolated (RHEED), and to grow up under these conditions.

[0013] Moreover, since this invention raises the quality of the semiconducting crystal which grows after 3 **** growth phase, in production of each device, it is important to prepare 3 **** growth phase before growth of the stratum functionale (for example, if it is semiconductor laser and is a barrier layer, a cladding layer, and FET channel layer etc.) which has close effect on the property of this device.

[0014]

[Example] Next, the example of this invention is explained using drawing 1. Although drawing 1 is the explanatory view showing the epitaxial structure of the MQW semiconductor laser produced based on this invention, this example is the same as that of the MQW semiconductor laser by the conventional example previously explained except for the point that there are 3 **** growth phase among drawing 1.

[0015] An n mold InP substrate and 2 one among drawing 1. Namely, the n mold InAlAs buffer layer of 0.5 micrometers of thickness, The n mold InAlAs cladding layer of 1 micrometer of thickness and 5 4 The p mold InAlGaAs-SCH layer of 0.15 micrometers of thickness, 6 Well width of face of 9nm, barrier width of face of 5nm, an InGaAs/InAlAs multiplex quantum well barrier layer with six wells, As for the p mold InAlGaAs-SCH layer of 0.15 micrometers of thickness, and 8, 7 is [the p mold InAlAs cladding layer of 2 micrometers of thickness and 9] the p+ mold InGaAs contact layers of 0.4 micrometers of thickness, and 3 is the InAlAs 3 **** growth phase of 30nm of thickness. Moreover, growth of all the semiconducting crystals except 3 **** growth phase 3 is performed where a crystal front face is maintained at 5 group stabilization side.

[0016] The threshold currents of the MQW semiconductor laser of this example were 0.8 kA/cm³. This value is the same level as the estimate from the threshold (1 kA/cm³) of the MQW semiconductor laser of an InP/InGaAsP system and ΔE_g value, and ΔE_c value, and it is shown that surface smoothness comparable as the case where an InP/InGaAsP crystal is grown up on an InP substrate, and crystallinity were acquired.

[0017] In addition, this invention can be similarly applied, not only when carrying out crystal growth of InGaAs/InAlAs on an InP substrate, but when carrying out crystal growth of AlGaAs/GaAs for example, on a GaAs substrate, and it can raise the surface smoothness of a crystal layer, and crystallinity further.

[0018] Moreover, although it is an example of application to MQW laser, the above-mentioned example can be applied to all the semiconductor devices constituted by InGaAs/InAlAs which grew on the InP substrate, or AlGaAs/GaAs which grew on the GaAs substrate, for example, can be applied also like electronic semiconductor devices, such as other semiconductor laser, a light receiving and emitting element or FET, and HEMT.

[0019] In the above-mentioned example, moreover, having formed the epitaxial growth phase 3 by 3 group stabilization side in the upper part of a buffer layer 2. In order to raise the surface smoothness of the SCH layers 5 and 7 which are important stratum functionale in this example, and a barrier layer 6, and crystallinity. Before growing up these important stratum functionale, it means introducing the epitaxial growth phase by 3 group stabilization side, and the introductory location of the epitaxial growth phase by 3 group stabilization side is not restricted to the above-mentioned example.

[0020]

[Effect of the Invention] Since the 3-5 group semiconducting crystal which is excellent in surface smoothness and crystallinity is producible with simply and sufficient repeatability according to this invention as explained above, the quality of a semiconductor device and improvement in a yield are attained.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the explanatory view showing the epitaxial structure of the MQW semiconductor laser produced based on this invention.

[Drawing 2] It is the explanatory view showing the epitaxial structure of the conventional MQW semiconductor laser.

[Description of Notations]

- 1 is an n mold InP substrate.
- 2 is an n mold InAlAs buffer layer.
- 3 is an InAlAs3 **** growth phase.
- 4 is an n mold InAlAs cladding layer.
- 5 is a p mold InAlGaAs-SCH layer.
- 6 is an InGaAs/InAlAs multiplex quantum well barrier layer.
- 7 is a p mold InAlGaAs-SCH layer.
- 8 is a p mold InAlAs cladding layer.
- 9 is a p+ mold InGaAs contact layer.
- 11 is an n mold InP substrate.
- 12 is an n mold InAlAs buffer layer.
- 13 is a superlattice buffer layer.
- 14 is an n mold InAlAs cladding layer.
- 15 is a p mold InAlGaAs-SCH layer.
- 16 is an InGaAs/InAlAs multiplex quantum well barrier layer.
- 17 is a p mold InAlGaAs-SCH layer.
- 18 is a p mold InAlAs cladding layer.
- 19 is a p+ mold InGaAs contact layer.

[Translation done.]

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技術表示箇所

H O 1 S 3/18

東京都千代田区丸の内2丁目6番1号 古河電気工業株式会社

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【特許請求の範囲】

【請求項1】 半導体基板上に、成長中の3-5族半導体結晶表面を5族安定化面に保持しつつ結晶成長を行う半導体薄膜の成長方法において、該半導体薄膜中に、結晶表面を3族安定化面に保持しつつ成長した膜厚1~200nmの薄膜結晶層を少なくとも1層設けることを特徴とする3-5族半導体薄膜の成長方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は、半導体基板上に高品質の3-5族半導体薄膜を結晶成長する方法に関するものである。

【0002】

【従来の技術】 InPに格子整合するInGaAs/InAlAs系の材料は、バンド構造が1.3~1.55μm帯の光通信用受発光素子に適している。また、InGaAsの電子移動度はGaAsと比較して2倍程度も大きいことから、次世代の電子デバイス材料として期待されている。このため現在、InP基板上に平坦性、結晶性に優れるInGaAs/InAlAsを結晶成長する方法が盛んに研究されている。

【0003】 一般に、MBE法、MOCVD法等で3-5族半導体を結晶成長する場合、5族元素の供給量が少ないと、蒸気圧の高い5族元素が結晶中から離脱して表面モホロジーが低下する。このため、3-5族半導体の結晶成長は、5族元素を過剰に供給して、成長中の結晶表面を5族安定化面に保った状態で行われる。

【0004】 ところが、InP基板上にInGaAs/InAlAsを結晶成長する場合は、成長時の結晶表面を5族安定化面に保持するのみでは結晶の平坦性、結晶性を十分高めることはできないという問題がある。具体的には、InGaAs/InAlAs量子井戸構造における価電子帯のバンドオフセット ΔE_c は $0.7\Delta E_g$ (バンドギャップエネルギー差 $\Delta E_g=0.70\text{eV}$) と、 ΔE_c が $0.4\Delta E_g$ ($\Delta E_g=0.59\text{eV}$) であるInP/InGaAsP量子井戸構造よりも高いことから、理論上、InGaAs/InAlAs系のMQW半導体レーザは、InP/InGaAsP系のMQW半導体レーザよりも低しきい値で発振すると考えられる。にもかかわらず、InP基板上に平坦性、結晶性に優れるInGaAs/InAlAs結晶を成長することが困難であるため、従来のInGaAs/InAlAs系のMQW半導体レーザのしきい値電流密度 (2.4kA/cm^2 程度) は、InP/InGaAsP系のMQW半導体レーザのしきい値 (1.0kA/cm^2 程度) と比較して劣っていた。

【0005】 ところで、InP基板上に成長するInGaAs/InAlAs結晶の平坦性、結晶性を改善する方法として、結晶層中に超格子バッファ層を導入する方法がある (マシューズ：特開昭48-20762)。図

2は、超格子バッファ層を導入したMQW半導体レーザのエピタキシャル構造を示す説明図である。

【0006】 図2中、11はn型InP基板、12は膜厚 $0.5\mu\text{m}$ のn型InAlAsバッファ層、14は膜厚 $1\mu\text{m}$ のn型InAlAsクラッド層、15は膜厚 $0.15\mu\text{m}$ のp型InAlGaAs-SCH層、16はウェル幅9nm、バリア幅5nm、ウェル数6のInGaAs/InAlAs多重量子井戸活性層、17は膜厚 $0.15\mu\text{m}$ のp型InAlGaAs-SCH層、18は膜厚 $0.4\mu\text{m}$ のp型InAlAsクラッド層、19は膜厚 $2\mu\text{m}$ のp⁺型InGaAsコンタクト層であり、13は膜厚2nmのInGaAsと膜厚2nmのInAlAsを各10層程度交互に積層した超格子バッファ層である。なお、この方法においても、成長中の結晶表面は常に5族安定化面に保たれている。

【0007】

【発明が解決しようとする課題】 しかし、超格子バッファ層を導入する従来の方法は、多数の超格子層を成長する必要があるため、膜厚や組成のコントロールが困難であるという問題点がある。また、図2に示すMQW半導体レーザのしきい値は 2.0kA/cm^2 とInP/InGaAsP系のMQW半導体レーザよりも劣っており、この方法により得られる結晶の平坦性、結晶性は不十分であることが示されている。

【0008】 本発明は、上記の問題点を解決して、簡易かつ安定に、半導体基板上に平坦性、結晶性の優れる3-5族半導体の結晶を成長する方法を提供することを目的とするものである。

【0009】

【課題を解決するための手段】 本発明は、成長中の結晶表面を3族安定化面に保持しつつ薄膜結晶を成長すると、該薄膜結晶中の3族元素のマイグレーションが活発となり、該薄膜結晶層の平坦性が促進される結果、その後成長する半導体結晶層の平坦性、結晶性が改善されとの発見に基づくものであり、半導体基板上に、成長中の3-5族半導体結晶表面を5族安定化面に保持しつつ結晶成長を行う半導体薄膜の成長方法において、該半導体薄膜中に、結晶表面を3族安定化面に保持しつつ成長した膜厚1~200nmの薄膜結晶層を少なくとも1層設けることを特徴とする半導体薄膜の成長方法である。

【0010】 本発明において、結晶表面を3族安定化面に保持しつつ成長した薄膜結晶層 (以下、3族面成長層という。) の膜厚を1nm以上に限定した理由は、3族面成長層の膜厚が薄くなると、3族元素のマイグレーションによる結晶の平坦化の度合いが不十分になる傾向があり、1nm以下の膜厚では本発明の効果が得られなくなるからであり、3族面成長層の膜厚を200nm以下に限定した理由は、膜厚を厚くすると5族元素の離脱による結晶の表面モホロジーの低下の程度が拡大する傾向

にあり、200nm以上の膜厚では、その後に成長する半導体結晶層の平坦性、結晶性が却って低下するためである。それ故、最も好ましい3族面成長層の膜厚は、10nm～50nmである。

【0011】また、3族面成長層を1層導入すれば、その後に成長する半導体結晶層の平坦性、結晶性は十分に向上するが、上記した膜厚の範囲であれば複数の3族面成長層を導入しても、その後に成長する半導体結晶層の平坦性、結晶性は低下することではなく、複数層の3族面成長層を導入することも本発明の範囲に含まれる。

【0012】なお、結晶表面を3族安定化面に制御する方法は公知である。すなわち、成長温度を上昇させ、あるいは5族元素供給量を減少させることにより成長層の表面を3族安定化面とすることが可能であり、反射型高エネルギー電子線回折装置(RHEED)により2×4超構造から4×2超構造に遷移する条件を把握して、該条件下で成長すると良い。

【0013】また、本発明は、3族面成長層の後に成長する半導体結晶の品質を向上させるものであるから、各デバイスの作製においては、該デバイスの特性に密接な影響を与える機能層(例えば半導体レーザであれば活性層やクラッド層、FETであればチャネル層等)の成長前に3族面成長層を設けることが肝要である。

【0014】

【実施例】次に、本発明の実施例を図1を用いて説明する。図1は、本発明に基づいて作製したMQW半導体レーザのエピタキシャル構造を示す説明図であるが、本実施例は、図1中、3が3族面成長層である点を除いて、先に説明した従来例によるMQW半導体レーザと同一である。

【0015】すなわち、図1中、1はn型InP基板、2は膜厚0.5μmのn型InAlAsバッファ層、4は膜厚1μmのn型InAlAsクラッド層、5は膜厚0.15μmのp型InAlGaAs-SCH層、6はウェル幅9nm、バリア幅5nm、ウェル数6のInGaAs/InAlAs多重量子井戸活性層、7は膜厚0.15μmのp型InAlGaAs-SCH層、8は膜厚2μmのp型InAlAsクラッド層、9は膜厚0.4μmのp⁺型InGaAsコンタクト層であり、3は膜厚30nmのInAlAs 3族面成長層である。また、3族面成長層3を除く全ての半導体結晶の成長は結晶表面を5族安定化面に保った状態で行われる。

【0016】本実施例のMQW半導体レーザのしきい値電流は0.8kA/cm²であった。この値はInP/InGaAsP系のMQW半導体レーザのしきい値(1kA/cm²)、及びΔE_g値、ΔE_c値からの推定値と同じレベルであり、InP基板上にInP/InGaAsP結晶を成長する場合と同程度の平坦性、結晶性が得られたことを示すものである。

【0017】なお、本発明はInP基板上にInGaAs/InAlAsを結晶成長する場合のみでなく、例えば、GaAs基板上にAlGaAs/GaAsを結晶成長する場合にも同様に適用することが可能であり、結晶層の平坦性、結晶性を更に向上させることができる。

【0018】また、上記実施例は、MQWレーザへの適用例であるが、InP基板上に成長したInGaAs/InAlAs、あるいは、GaAs基板上に成長したAlGaAs/GaAsにより構成される全ての半導体デバイスに適用することができ、例えば他の半導体レーザや受発光素子、あるいは、FET、HEMT等の電子半導体素子にも同様に適用することができる。

【0019】また、上記実施例において、3族安定化面によるエピタキシャル成長層3をバッファ層2の上部に設けたのは、該実施例における重要な機能層であるSCH層5、7及び活性層6の平坦性、結晶性を高めるため、これらの重要な機能層を成長する以前に3族安定化面によるエピタキシャル成長層を導入することを意図したものであり、3族安定化面によるエピタキシャル成長層の導入位置は上記実施例に限られない。

【0020】

【発明の効果】以上説明したように、本発明によれば平坦性、結晶性に優れる3-5族半導体結晶を簡易かつ再現性良く作製できるため、半導体デバイスの品質及び歩留の向上が達成される。

【図面の簡単な説明】

【図1】本発明に基づいて作製したMQW半導体レーザのエピタキシャル構造を示す説明図である。

【図2】従来のMQW半導体レーザのエピタキシャル構造を示す説明図である。

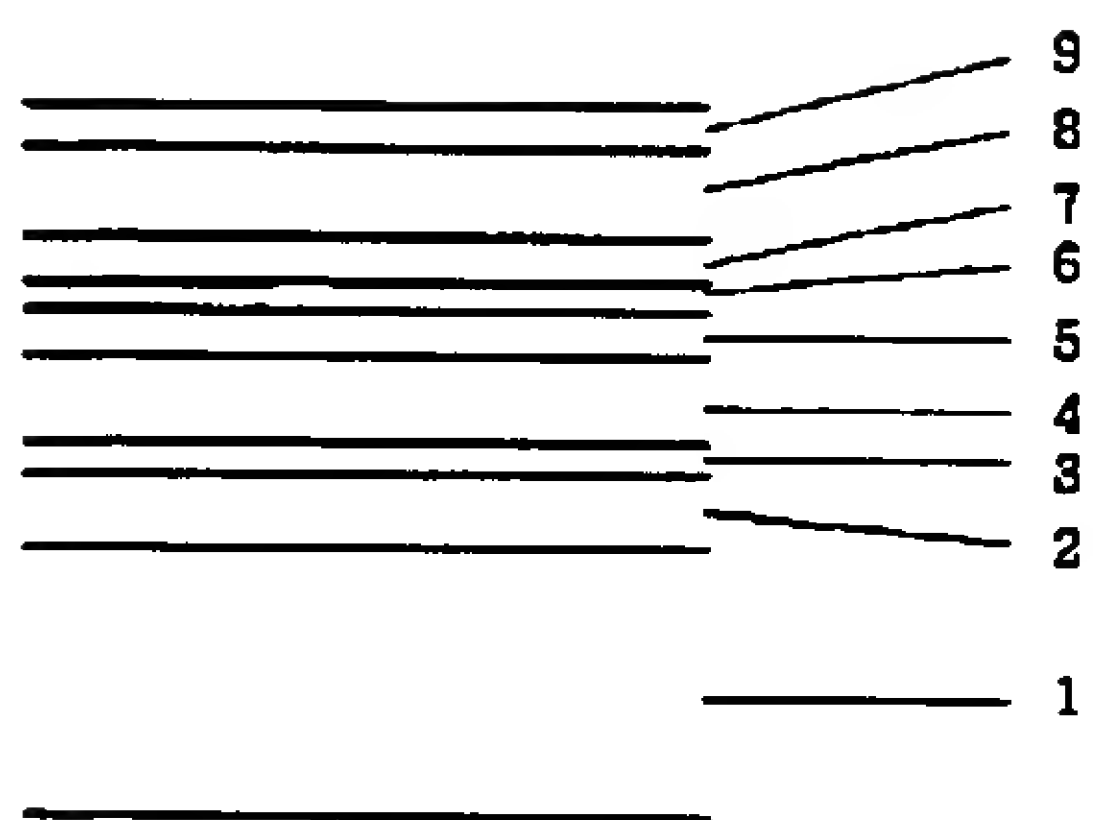
【符号の説明】

- 1はn型InP基板
- 2はn型InAlAsバッファ層
- 3はInAlAs 3族面成長層
- 4はn型InAlAsクラッド層
- 5はp型InAlGaAs-SCH層
- 6はInGaAs/InAlAs多重量子井戸活性層
- 7はp型InAlGaAs-SCH層
- 8はp型InAlAsクラッド層
- 9はp⁺型InGaAsコンタクト層
- 11はn型InP基板
- 12はn型InAlAsバッファ層
- 13は超格子バッファ層
- 14はn型InAlAsクラッド層
- 15はp型InAlGaAs-SCH層
- 16はInGaAs/InAlAs多重量子井戸活性層
- 17はp型InAlGaAs-SCH層
- 18はp型InAlAsクラッド層
- 19はp⁺型InGaAsコンタクト層

(4)

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【図1】



【図2】

